National Semiconductor

January 2003

ADC10030
10-Bit, 30 MSPS, 125 mW A/D Converter with Internal Sample and Hold

General Description

The ADC10030 is a low power, high performance CMOS analog-to-digital converter that digitizes signals to 10 bits resolution at sampling rates up to 30 Msps while consuming a typical 125 mW from a single 5V supply. Reference force and sense pins allow the user to connect an external reference buffer amplifier to ensure optimal accuracy. No missing codes is guaranteed over the full operating temperature range. The unique two-stage architecture achieves 9.1 Effective Bits with a 15 MHz input signal and a 30 MHz clock frequency. Output formatting is straight binary coding.

To ease interfacing to 3V systems, the digital I/O power pins of the ADC10030 can be tied to a 3V power source, making the outputs 3V compatible. When not converting, power consumption can be reduced by pulling the PD (Power Down) pin high, placing the converter into a low power standby state, where it typically consumes less than 4 mW. The ADC10030's speed, resolution and single supply operation makes it well suited for a variety of applications in video, imaging, communications, multimedia and high speed data acquisition. Low power, single supply operation ideally suit the ADC10030 for high speed portable applications, and its speed and resolution are ideal for charge coupled device (CCD) input systems.

The ADC10030 comes in a space saving 32-pin TQFP and operates over the industrial ($-40^{\circ}C \le T_A \le +85^{\circ}C$) temperature range.

Features

- Internal Sample-and-Hold
- Single +5V Operation
- Low Power Standby Mode
- Guaranteed No Missing Codes
- TRI-STATE Outputs
- TTL/CMOS or 3V Logic Input/Output Compatible

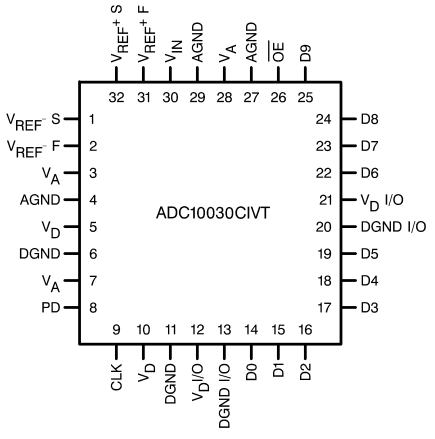
Key Specifications

Resolution	10 Bits
Conversion Rate	30 Msps
ENOB @ 15 MHz Input	9.1 Bits (typ)
DNL	0.40 LSB (typ)
Conversion Latency	2 Clock Cycles
PSRR	56 dB
Power Consumption	125 mW (typ)
Low Power Standby Mode	<3.5 mW (typ)

Applications

- Digital Video
- Communications
- Document Scanners
- Medical Imaging
- Electro-Optics
- Plain Paper Copiers
- CCD Imaging

Connection Diagram



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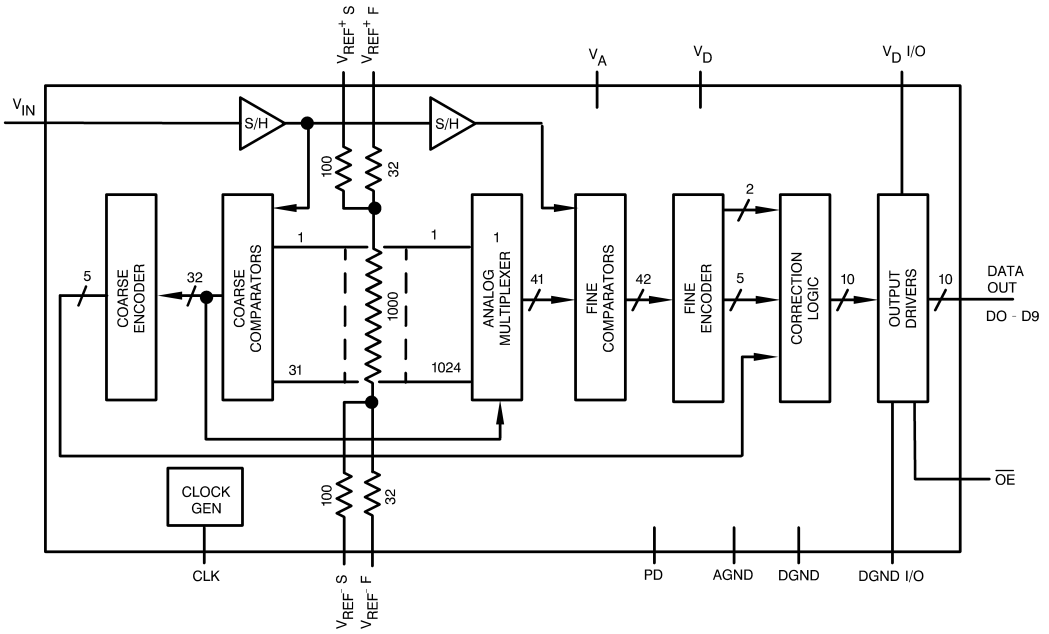
Ordering Information

Commercial Temperature Range ($-40^{\circ}C \leq T_A \leq +85^{\circ}C$)	NS Package
ADC10030CIVT	TQFP

Block Diagram



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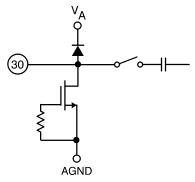
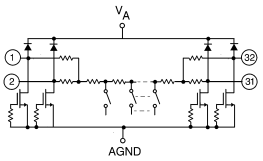
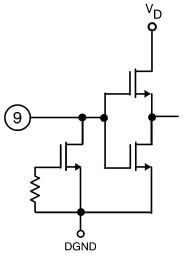
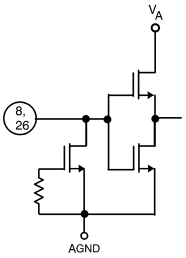
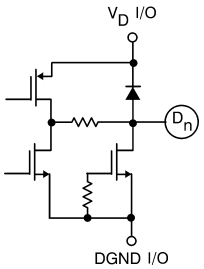
Pin Descriptions and Equivalent Circuits

Pin No.	Symbol	Equivalent Circuit	Description
30	V_{IN}		Analog Input signal to be converted. Conversion range is V_{REF+} S to V_{REF-} S.
31	V_{REF+} F		Analog input that goes to the high side of the reference ladder of the ADC. This voltage should force V_{REF+} S to be in the range of 2.6V to 3.8V.
32	V_{REF+} S		Analog output used to sense the voltage near the top of the ADC reference ladder.
2	V_{REF-} F		Analog input that goes to the low side of the reference ladder of the ADC. This voltage should force $V_{REF\_}$ S to be in the range of 1.7V to 2.8V.
1	V_{REF-} S		Analog output used to sense the voltage near the bottom of the ADC reference ladder.
9	CLK		Converter digital clock input. V_{IN} is sampled on the falling edge of CLK input.
8	PD		Power Down input. When this pin is high, the converter is in the Power Down mode and the data output pins are in a high impedance state.
26	$\overline{OE}$		Output Enable pin. When this pin and the PD pin are low, the output data pins are active. When this pin or the PD pin is high, the data output pins are in a high impedance state.
14 thru 19 and 22 thru 25	D0–D9		Digital Output pins providing the 10-bit conversion results. D0 is the LSB, D9 is the MSB. Data is acquired on the falling edge of the CLK input and valid data is present 2.0 clock cycles plus t_{OD} later.
3, 7, 28	V_A		Positive analog supply pins. These pins should be connected to a clean, quiet voltage source of +5V. V_A and V_D should have a common supply and be separately bypassed with 10 µF to 50 µF capacitors in parallel with 0.1 µF capacitors.
5, 10	V_D		Positive digital supply pins. These pins should be connected to a clean, quiet voltage source of +5V. V_A and V_D should have a common supply and be separately bypassed with 10 µF to 50 µF capacitors in parallel with 0.1 µF capacitors.

Pin Descriptions and Equivalent Circuits (Continued)

Pin No.	Symbol	Equivalent Circuit	Description
12, 21	V_D I/O		Positive supply pins for the digital output drivers. These pins should be connected to a clean, quiet voltage source of +3V to +5V and be separately bypassed with 10 µF to 50 µF capacitors.
4, 27, 29	AGND		The ground return for the analog supply. AGND and DGND should be connected together close to the ADC10030 package.
6, 11	DGND		The ground return for the digital supply. AGND and DGND should be connected together close to the ADC10030 package.
13, 20	DGND I/O		The ground return of the digital output drivers.

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Positive Supply Voltage (V = V_A = V_D)	6.5V
Voltage on Any Pin	−0.3V to (V_A or V_D +0.3V)
Input Current at Any Pin (Note 3)	±25 mA
Package Input Current (Note 3)	±50 mA
Package Dissipation at T_A = 25˚C	See (Note 4)
ESD Susceptibility (Note 5)	
Human Body Model	1500V
Machine Model	200V
Soldering Temp., Infrared, 10 sec. (Note 6)	235˚C
Storage Temperature	−65˚C to +150˚C

Operating Ratings (Notes 1, 2)

Operating Temperature Range	$-40^{\circ}C \le T_A \le +85^{\circ}C$
V_A, V_D Supply Voltage	+4.75V to +5.5V
V_D I/O Supply Voltage	+2.7V to 5.5V
V_{IN} Voltage Range	1.7V to (V_A−1.2V)
V_{REF}+ Voltage Range	2.6V to (V_A−1.2V)
V_{REF}− Voltage Range	1.7V to 2.8V
PD, CLK, $\overline{OE}$ Voltage Range	−0.3V to +5.5V

Converter Electrical Characteristics

The following specifications apply for V_A = +5.0V_{DC}, V_D = 5.0V_{DC}, V_D I/O = +5.0V_{DC}, V_{REF}+ = +3.5V_{DC}, V_{REF}− = +1.75V_{DC}, C_L = 20 pF, f_{CLK} = 27 MHz, R_S = 50Ω. **Boldface limits apply for T_A = T_{MIN} to T_{MAX}:** all other limits T_A = 25˚C (Note 7)

Symbol	Parameter	Conditions	Typical (Note 8)	Limits (Note 9)	Units
Static Converter Characteristics					
INL	Integral Non-Linearity		±0.45	**±1.0**	LSB(max)
DNL	Differential-Non-Linearity		±0.40	**±0.95**	LSB(max)
	Resolution with No Missing Codes			**10**	Bits
	Zero Scale Offset Error		−4		mV
	Full-Scale Offset Error		+3		mV
Dynamic Converter Characteristics					
ENOB	Effective Number of Bits	f_{IN} = 1.0 MHz	9.6		Bits
		f_{IN} = 4.43 MHz	9.4		Bits
		f_{IN} = 13.5 MHz	9.4	**8.6**	Bits
		f_{IN} = 4.43 MHz, f_{CLK} = 30 MHz	9.3		Bits
		f_{IN} = 15.0 MHz, f_{CLK} = 30 MHz	9.1		Bits
S/(N+D)	Signal-to-Noise Plus Distortion Ratio	f_{IN} = 1.0 MHz	60		dB
		f_{IN} = 4.43 MHz	59		dB
		f_{IN} = 13.5 MHz	58	**53.5**	dB
		f_{IN} = 4.43 MHz, f_{CLK} = 30 MHz	58		dB
		f_{IN} = 15.0 MHz, f_{CLK} = 30 MHz	57		dB
SNR	Signal-to-Noise Ratio	f_{IN} = 1.0 MHz	60		dB
		f_{IN} = 4.43 MHz	59		dB
		f_{IN} = 13.5 MHz	59	**54**	dB
		f_{IN} = 4.43 MHz, f_{CLK} = 30 MHz	59		dB
		f_{IN} = 15.0 MHz, f_{CLK} = 30 MHz	58		dB
THD	Total Harmonic Distortion	f_{IN} = 1.0 MHz	−72		dB
		f_{IN} = 4.43 MHz	−69		dB
		f_{IN} = 13.5 MHz	−66	**−61**	dB
		f_{IN} = 4.43 MHz, f_{CLK} = 30 MHz	−64		dB
		f_{IN} = 15.0 MHz, f_{CLK} = 30 MHz	−61		dB
SFDR	Spurious Free Dynamic Range	f_{IN} = 1.0 MHz	73		dB
		f_{IN} = 4.43 MHz	71		dB
		f_{IN} = 13.5 MHz	68		dB
		f_{IN} = 4.43 MHz, f_{CLK} = 30 MHz	66		dB
		f_{IN} = 15.0 MHz, f_{CLK} = 30 MHz	62		dB

Converter Electrical Characteristics (Continued)

The following specifications apply for V_A = +5.0V_{DC}, V_D = 5.0V_{DC}, V_D I/O = +5.0V_{DC}, V_{REF}+ = +3.5V_{DC}, V_{REF}− = +1.75V_{DC}, C_L = 20 pF, f_{CLK} = 27 MHz, R_S = 50Ω. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}:** all other limits T_A = 25˚C (Note 7)

Symbol	Parameter	Conditions	Typical (Note 8)	Limits (Note 9)	Units
	Overrange Output Code	$V_{IN} > V_{REF}$+		**1023**	
	Underrange Output Code	$V_{IN} < V_{REF}$−			
BW	Full Power Bandwidth		150		MHz
PSRR	Power Supply Rejection Ratio	Change in Full Scale with 4.5V to 5.5V Supply Change	56		dB

Reference, DC, and Logic Electrical Characteristics

The following specifications apply for V_A = +5.0V_{DC}, V_D = +5.0V_{DC}, V_D I/O = +5.0V_{DC}, V_{REF}+ = +3.5V_{DC}, V_{REF}− = +1.75V_{DC}, C_L = 20 pF, f_{CLK} = 27 MHz, R_S = 50Ω. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}:** all other limits T_A = 25˚C (Note 7)

Symbol	Parameter	Conditions	Typical (Note 8)	Limits (Note 9)	Units
Reference and Analog Input Characteristics					
V_{IN}	Analog Input Range		1.75 3.5	**1.6** **3.8**	V(min) V(max)
C_{IN}	Analog V_{IN} Input Capacitance		5		pF
I_{IN}	Input Leakage Current		10		µA
R_{REF}	Reference Ladder Resistance		1000	**850** **1150**	Ω(min) Ω(max)
V_{REF}+	Positive Reference Voltage		3.5	**3.8**	V(max)
V_{REF}−	Negative Reference Voltage		1.75	**1.6**	V(min)
(V_{REF}+) − (V_{REF}−)	Total Reference Voltage		1.75	**1.0** **2.2**	V(min) V(max)
CLK, $\overline{OE}$, PD, Digital Input Characteristics					
V_{IH}	Logical “1” Input Voltage	V_D = 5.5V		**2.0**	V(min)
V_{IL}	Logical “0” Input Voltage	V_D = 4.5V		**1.0**	V(max)
I_{IH}	Logical “1” Input Current	$V_{IH} = V_D$	10		µA
I_{IL}	Logical “0” Input Current	V_{IL} = DGND	−10		µA
DB0–DB9 Digital Output Characteristics					
V_{OH}	Logical “1” Output Voltage	V_D I/O = +4.5V, I_{OUT} = −0.5 mA V_D I/O = +2.7V, I_{OUT} = −0.5 mA		**4.0** **2.4**	V(min) V(min)
V_{OL}	Logical “0” Output Voltage	V_D I/O = +4.5V, I_{OUT} = −1.6 mA V_D I/O = +2.7V, I_{OUT} = −1.6 mA		**0.4** **0.4**	V(max) V(max)
I_{OZ}	TRI-STATE Output Current	V_{OUT} = DGND $V_{OUT} = V_D$	−10 10		µA µA
I_{OS}	Output Short Circuit Current	V_D I/O = 3V	±12		mA
		V_D I/O = 5V	±25		mA
Power Supply Characteristics					
I_A	Analog Supply Current	PD = LOW, Ladder Current not included PD = HIGH, Ladder Current not included	17.6 0.5		mA(max) mA
I_D + I_D I/O	Digital Supply Current	PD = LOW, Ladder Current not included PD = HIGH, Ladder Current not included	6.6 0.2		mA(max) mA

Reference, DC, and Logic Electrical Characteristics (Continued)

The following specifications apply for V_A = +5.0V_{DC}, V_D = +5.0V_{DC}, V_D I/O = +5.0V_{DC}, V_{REF}+ = +3.5V_{DC}, V_{REF}− = +1.75V_{DC}, C_L = 20 pF, f_{CLK} = 27 MHz, R_S = 50Ω. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}:** all other limits T_A = 25˚C (Note 7)

Symbol	Parameter	Conditions	Typical (Note 8)	Limits (Note 9)	Units
P_D	Power Consumption	PD = LOW	121	**130**	mW(max)
		PD = HIGH	3.5		
		PD = LOW, f_{CLK} = 30 MHz	125		mW

AC Electrical Characteristics

The following specifications apply for V_A = +5.0V_{DC}, V_D = +5.0V_{DC}, V_D I/O = 5.0V_{DC}, V_{REF}+ = +3.5V_{DC}, V_{REF}− = +1.75V_{DC}, C_L = 20 pF, f_{CLK} = 27 MHz, R_S = 50Ω. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}:** all other limits T_A = 25˚C (Note 7)

Symbol	Parameter	Conditions	Typical (Note 8)	Limits (Note 9)	Units (Limits)
f_{CLK1}	Maximum Clock Frequency		27	**30**	MHz
f_{CLK2}	Minimum Clock Frequency		1		MHz
t_{CH}	Clock High Time			**16.5**	ns(min)
t_{CL}	Clock Low Time			**16.5**	ns(min)
	Duty Cycle		50	**45** **55**	%(min) %(max)
	Pipeliine Delay (Latency)			**2.0**	Clock Cycles
t_{rc}, t_{fc}	Clock Input Rise and Fall Time			**4**	ns(max)
t_r, t_f	Output Rise and Fall Times		10		ns
t_{OD}	Fall of CLK to Data Valid		20	**25**	ns(max)
t_{OH}	Output Data Hold Time		12		ns
t_{DIS}	Rising Edge of $\overline{OE}$ to TRI-STATE™	From Output High, 2 kΩ to Ground	25		ns
		From Output Low, 2 kΩ to V_D I/O	18		ns
t_{EN}	Falling Edge of $\overline{OE}$ to Valid Data	1 kΩ to V_{CC}	25		ns
t_{VALID}	Data Valid Time		27		ns
t_{AD}	Aperture Delay		4		ns
t_{AJ}	Aperture Jitter		<30		ps
	Full Scale Step Response	t_r = 10 ns	1		conversion
	Overrange Recovery Time	V_{IN} Step from (V_{REF}+ +100 mV) to (V_{REF}−)	1		conversion
t_{WU}	PD Low to ½ LSB Accurate Conversion (Wake-Up Time)		700		ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to GND = AGND = DGND = 0V, unless otherwise specified.

Note 3: When the input voltage at any pin exceeds the power supplies (V_{IN} < GND or V_{IN} > V_A or V_D), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two.

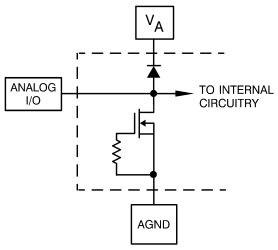
Note 4: The absolute maximum junction temperature ($T_J$max) for this device is 150˚C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A), and can be calculated using the formula P_DMAX = ($T_J$max − T_A)/θ_{JA}. In the 32-pin TQFP, θ_{JA} is 69˚C/W, so P_DMAX = 1,811 mW at 25˚C and 942 mW at the maximum operating ambient temperature of 85˚C. Note that the power dissipation of this device under normal operation will typically be about 137 mW (125 mW quiescent power + 2 mW reference ladder power +10 mW due to 1 TTL load on each digital output). The values for maximum power dissipation listed above will be reached only when the ADC10030 is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions should always be avoided.

Note 5: Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through ZERO Ω.

Note 6: The 235˚C reflow temperature refers to infared reflow. For Vapor Phase Reflow (VPR), the following conditions apply: Maintain the temperature at the top of the package body above 183˚C for a minimum 60 seconds. The temperature measured on the package body must not exceed 220˚C. Only one excursion above 183˚C is allowed per reflow cycle.

Note 7: The inputs are protected as shown below. Input voltage magnitudes up to 300 mV beyond the supply rails will not damage this device. However, errors in the A/D conversion can occur if the input goes above V_A or below AGND by more than 300 mV.

AC Electrical Characteristics (Continued)



ANALOG PIN PROTECTION

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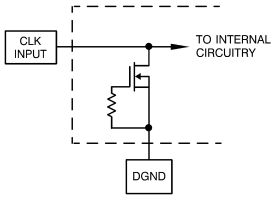

CLOCK PIN PROTECTION

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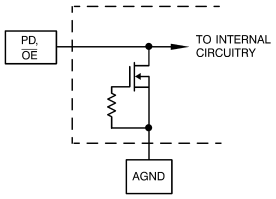

CLOCK PIN PROTECTION

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Note 8: Typical figures are at T_J = 25˚C, and represent most likely parametric norms.

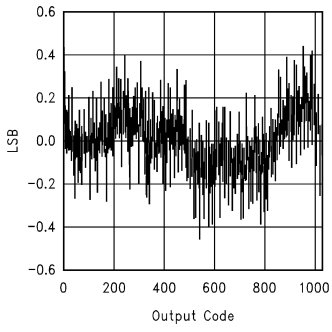
Note 9: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 10: When the input signal is between V_{REF}+ and (V_A + 300 mV), the output code will be 3FFh, or all 1s. When the input signal is between –300 mV and V_{REF}–, the output code will be 000h, or all 0s.

Typical Performance Characteristics

$V_A = V_D = V_D$ I/O = 5V, T_A = 25˚C, f_{IN} = 4.4 MHz, f_{CLK} = 27 MHz, unless otherwise specified.

Typical INL



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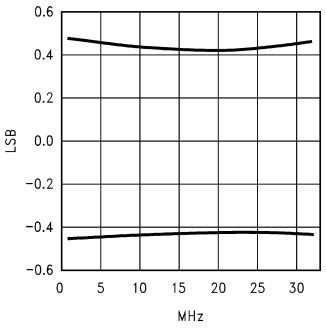
INL vs f_{CLK}



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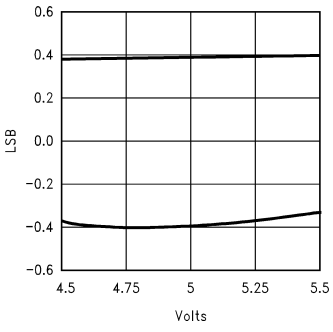
INL vs V_A



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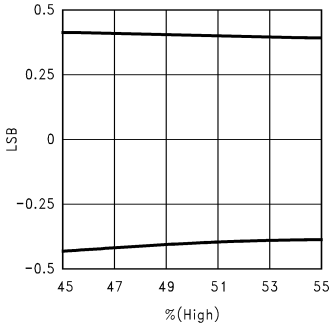
INL vs Clock Duty Cycle



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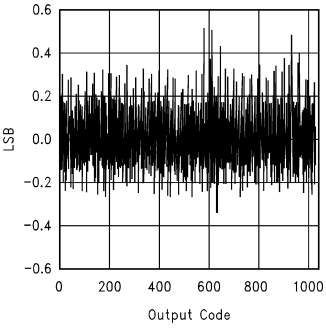
Typical DNL



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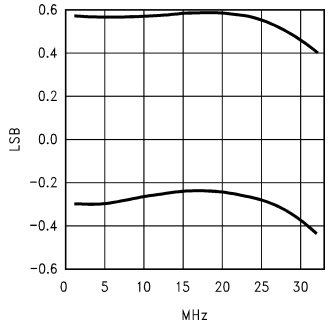
DNL vs f_{CLK}



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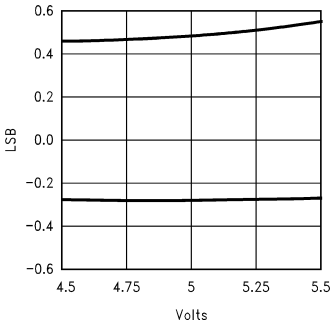
DNL vs V_A



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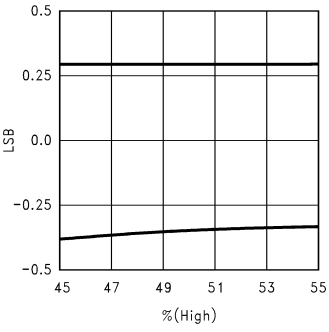
DNL vs Clock Duty Cycle



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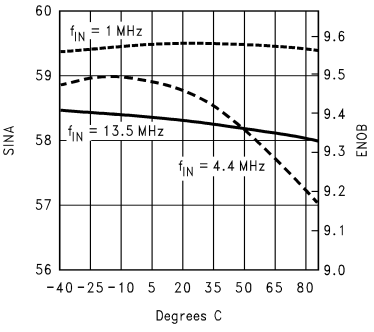
SINAD & ENOB vs Temperature and f_{IN}



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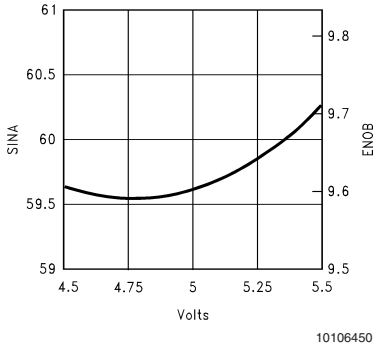
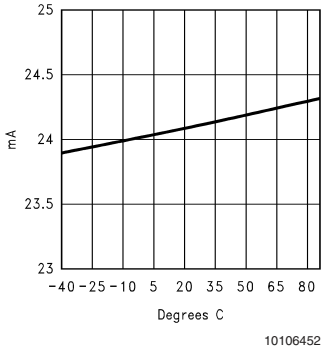
Typical Performance Characteristics $V_A = V_D = V_D$ I/O = 5V, T_A = 25˚C, f_{IN} = 4.4 MHz, f_{CLK} = 27 MHz, unless otherwise specified. (Continued)

SINAD & ENOB vs V_A



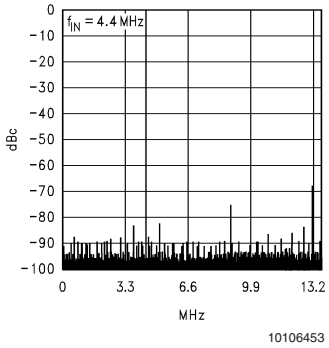
10106450

$I_A + I_D$ vs Temparature



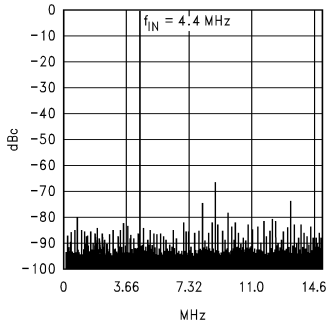
10106452

Spectral Response at 27 MSPS



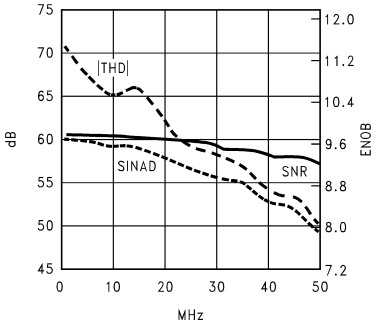
10106453

Spectral Response at 30 MSPS



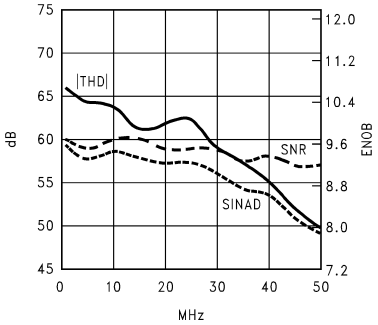
10106454

Dynamics at 27 MSPS



10106455

Dynamics at 30 MSPS



10106456

Specification Definitions

APERTURE JITTER is the variation in aperture delay from sample to sample. Aperture jitter shows up as input noise.

APERTURE DELAY See Sampling Delay.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise plus Distortion Ratio (S/N+D or SINAD). ENOB is defined as (SINAD −1.76) / 6.02.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its 1 MHz value for a full scale input. The test is performed with f_{IN} equal to 100 kHz plus integral multiples of f_{CLK}. The input frequency at which the output is −3 dB relative to the 1 MHz input signal is the full power bandwidth.

FULL SCALE (FS) INPUT RANGE of the ADC is the input range of voltages over which the ADC will digitize that input. For $V_{REF}+$ = 3.5V and $V_{REF}-$ = 1.5V, FS = ($V_{REF}+$) − ($V_{REF}-$) = 2.0V.

FULL SCALE OFFSET ERROR is a measure of how far the last code transition is from the ideal 1½ LSB below $V_{REF}+$ and is defined as V_{1023} +1.5 LSB − $V_{REF}+$, where V_{1023} is the voltage at which the transition from code 1022 to 1023 occurs.

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from negative full scale (½ LSB below the first code transition) through positive full scale (1½ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value.

OUTPUT DELAY is the time delay after the fall of the input clock before the data update is present at the output pins.

OUTPUT HOLD TIME is the length of time that the output data is valid after the fall of the input clock.

PIPELINE DELAY (LATENCY) is the number of clock cycles between initiation of conversion and when that data is presented to the output driver stage. Data for any given sample is available by the Pipeline Delay plus the Output Delay after that sample is taken. New data is available at every clock cycle, but the data lags the conversion by the Pipeline Delay plus the Output Delay.

PSRR (POWER SUPPLY REJECTION RATIO) is the ratio of the change in dc power supply voltage to the resulting change in Full Scale Error, expressed in dB.

SAMPLING (APERTURE) DELAY or APERTURE TIME is that time required after the fall of the clock input for the sampling switch to open. The sample is effectively taken this amount of time after the fall of the clock input.

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the RMS value of the input signal to the RMS value of other spectral components below half the clock frequency, not including harmonics or dc.

SIGNAL TO NOISE PLUS DISTORTION (S/(N+D) or SINAD) is the ratio, expressed in dB, of the RMS value of the input signal to the RMS value of all of the other spectral components below half the clock frequency, including harmonics but excluding dc.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB or dBc, between the RMS value of the input signal and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input.

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dB, of the RMS total of the first six harmonic components, to the RMS value of the input signal.

ZERO SCALE OFFSET ERROR is the difference between the ideal input voltage (½ LSB) and the actual input voltage that just causes a transition from an output code of zero to an output code of one.

Timing Diagram

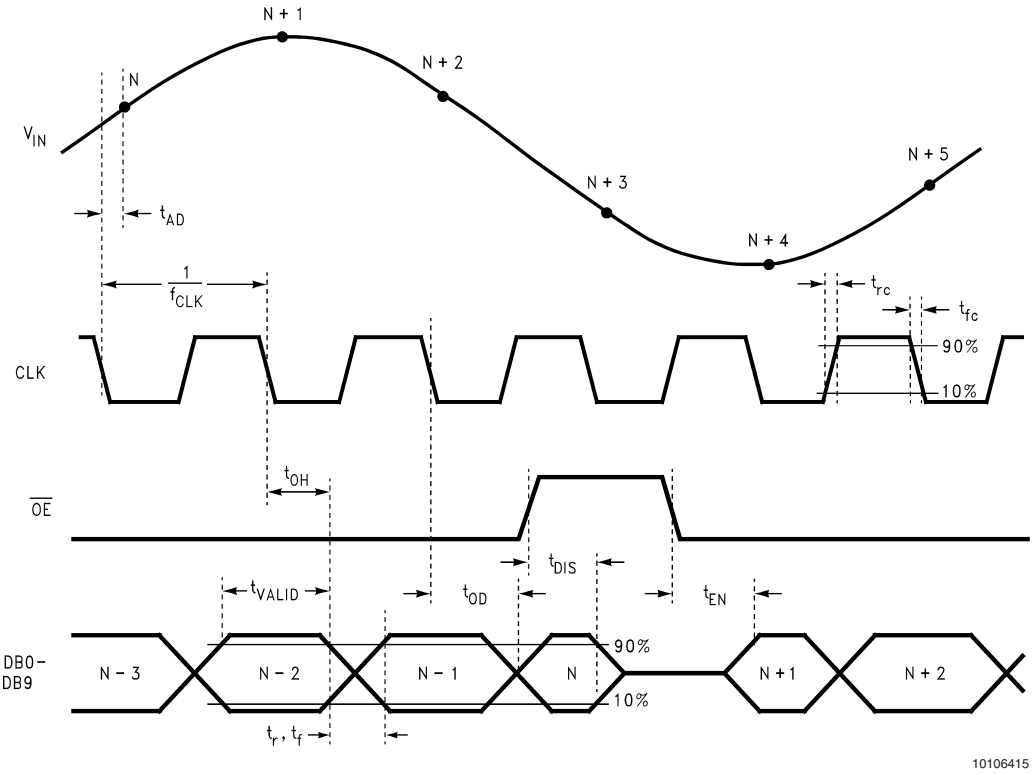


FIGURE 1. ADC10030 Timing Diagram

Test Circuits

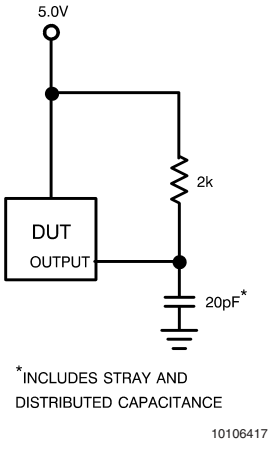


FIGURE 2. AC Test Circuit

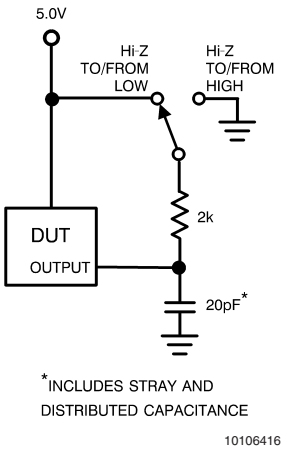


FIGURE 3. t_{EN}, t_{DIS} Test Circuit

Functional Description

The ADC10030 maintains excellent dynamic performance for input signals up to and exceeding half the clock frequency. The use of an internal sample-and-hold amplifier (SHA) enables sustained dynamic performance for signals of input frequency beyond the clock rate, lowers the converter's input capacitance and reduces the number of external components required.

The analog signal at V_{IN} that is within the voltage range set by V_{REF}+ S and V_{REF}− S are digitized to ten bits at up to 30 MSPS. Input voltages below V_{REF}− S will cause the output word to consist of all zeroes. Input voltages above V_{REF}+ S will cause the output word to consist of all ones. V_{REF}+ S has a range of 2.6V to 3.8V, while V_{REF}− S has a range of 1.7V to 2.8V. V_{REF}+ S should always be at least 1.0V more positive than V_{REF}− S.

Data is acquired at the falling edge of the clock and the digital equivalent of that data is available at the digital outputs 2.0 clock cycles plus t_{OD} later. The ADC10030 will convert as long as the clock signal is present at pin 9 and the PD pin is low. The Output Enable pin ($\overline{OE}$), when low, enables the output pins. The digital outputs are in the high impedance state when the $\overline{OE}$ pin or the PD pin is high.

Applications Information

1.0 THE ANALOG INPUT

The analog input of the ADC10030 is a switch (transmission gate) followed by a switched capacitor amplifier. The capacitance seen at the input changes with the clock level, appearing as about 3 pF when the clock is low, and about 5 pF when the clock is high. This small change in capacitance can be reasonably assumed to be a fixed capacitance. Care should be taken to avoid driving the input beyond the supply rails, even momentarily, as during power-up.

The LMH6702 has been found to be a good device to drive the ADC10030 because of its wide bandwidth, low distortion and minimal Differential Gain and Differential Phase. The LMH6702 performs best with a feedback resistor of about 100Ω.

Care should be taken to keep digital noise out of the analog input circuitry to maintain highest noise performance.

2.0 REFERENCE INPUTS

Note: Throughout this data sheet reference is made to V_{REF}+ and to V_{REF}−. These refer to the internal voltage across the reference ladder and are, nominally, V_{REF}+ S and V_{REF}− S, respectively.

Figure 4 shows a simple reference biasing scheme with minimal components. While this circuit might suffice for some applications, it does suffer from thermal drift because the external resistor at pin 2 will have a different temperature coefficient than the on-chip resistors. Also, the on-chip resistors, while well matched to each other, will have a large tolerance compared with any external resistors, causing the value of V_{REF}+ and V_{REF}− to be somewhat variable. No d.c. current should be allowed to flow through pin 1 or 32 or linearity errors will result near the zero scale and full scale ends of the signal excursion. The sense pins were designed to be used with high impedance opamp inputs for high accuracy biasing.

The V_{REF}+ F and V_{REF}− F pins should each be bypassed to AGND with 10 µF tantalum or electrolytic capacitors and 0.1 µF ceramic capacitors.

The circuit of *Figure 5* is an improvement over the circuit of *Figure 4* in that the positive end of the reference ladder is defined with a reference voltage. This reduces problems of high reference variability and thermal drift.

In addition to the usual reference inputs, the ADC10030 has two sense outputs for precision control of the ladder voltages. These sense outputs (V_{REF}+ S and V_{REF}− S) compensate for errors due to IR drops between the source of the reference voltages and the ends of the reference ladder itself.

With the addition of two op-amps, the voltages at the top and bottom of the reference ladder can be forced to the exact value desired, as shown in *Figure 6*.

Applications Information (Continued)

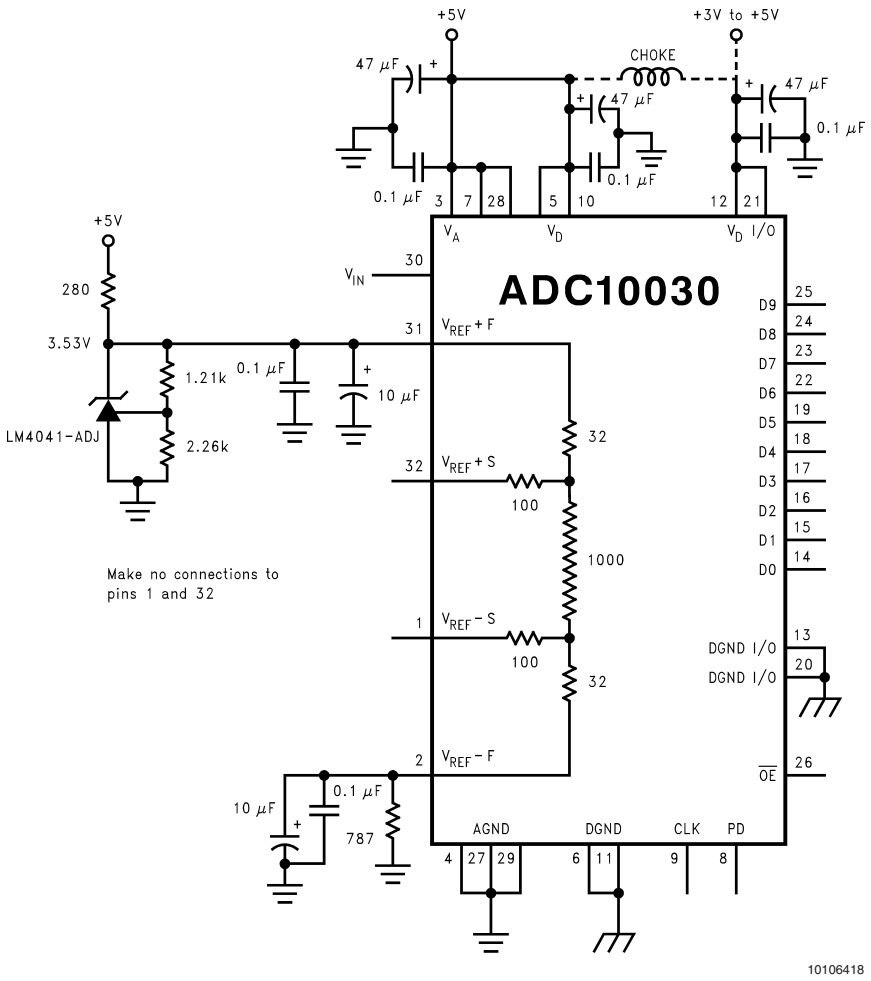


FIGURE 4. Simple, Low Component Count Reference Biasing

Applications Information (Continued)

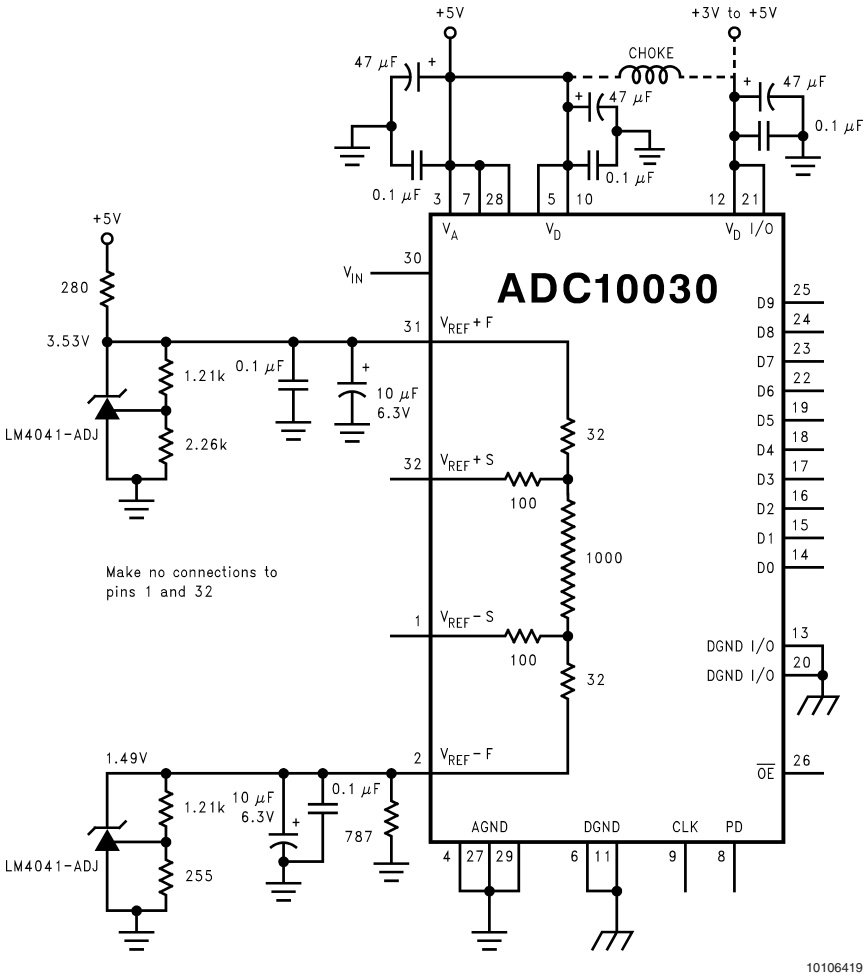


FIGURE 5. Improved Low Component Count Reference Biasing

The circuit of *Figure 6* may be used if it is desired to obtain precise reference voltages. The LMC6082 in this circuit was chosen for its low offset voltage, low voltage rail-to-rail capability and low cost.

Since the current flowing through the sense lines (those lines associated with V_{REF}+ S and V_{REF}− S) is essentially zero, there is negligible voltage drop across any resistance in series with these sense pins and the voltage at the inverting input of the op-amp accurately represents the voltage at the top (or bottom) of the ladder. The op-amp drives the force input, forcing the voltage at the ends of the ladder to equal the voltage at the op-amp's non-inverting input, plus any offset voltage. For this reason, op-amps with low V_{OS}, such as the LMC6081 and LMC6082, should be used for this application.

Voltages at the reference sense pins (V_{REF}+ S and V_{REF}− S) should be within the range specified in the Operating Ratings table (2.6V to 3.8V for V_{REF}+ and 1.7V to V_A - 1.2V for V_{REF}−). Any device used to drive the reference pins should be able to source sufficient current into the V_{REF}+ F pin and sink sufficient current from the V_{REF}− F pin when the ladder is at its minimum value of 850Ω.

The reference voltage at the top of the ladder (V_{REF}+) may take on values as low as 1.0V above the voltage at the bottom of the ladder (V_{REF}−) and as high as (V_A – 1.2V). The voltage at the bottom of the ladder (V_{REF}−) may take on values as low as 1.7V and as high as 2.8V. However, to minimize noise effects and ensure accurate conversions, the total reference voltage range (V_{REF}+ – V_{REF}−) should be a minimum of 1.0V and a maximum of 2.2V.

Applications Information (Continued)

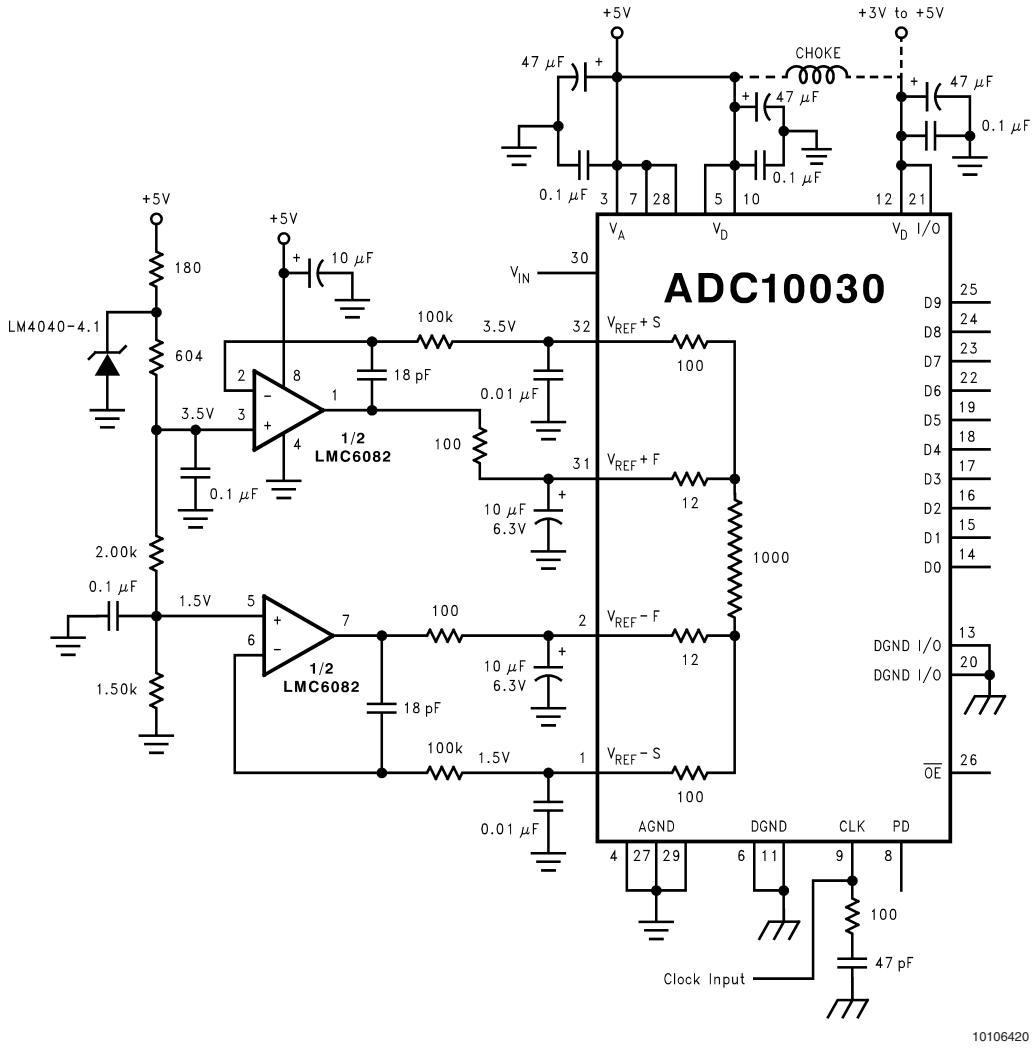


FIGURE 6. Setting Precision Reference Voltages

3.0 POWER SUPPLY CONSIDERATIONS

A/D converters draw sufficient transient current to corrupt their own power supplies if not adequately bypassed. A 10 µF to 50 µF tantalum or aluminum electrolytic capacitor should be placed within an inch (2.5 centimeters) of the A/D power pins, with a 0.1 µF ceramic chip capacitor placed as close as possible to each of the converter's power supply pins. Leadless chip capacitors are preferred because they have low lead inductance.

While a single voltage source should be used for the analog and digital supplies of the ADC10030, this supply should **not** be the supply that is used for other digital circuitry on the board.

As is the case with all high-speed converters, the ADC10030 should be assumed to have little high frequency power supply rejection. A clean analog power source should be used.

No pin should ever have a voltage on it that is more than 300 mV in excess of the supply voltages or below ground, not even on a transient basis. This can be a problem upon application of power to a circuit. Be sure that the supplies to circuits driving the CLK, PD, $\overline{OE}$, analog input and reference pins do not come up any faster than does the voltage at the ADC10030 power pins.

4.0 THE ADC10030 CLOCK

Although the ADC10030 is tested and its performance is guaranteed with a 27 MHz clock, it typically will function with clock frequencies from 1 MHz to 30 MHz. Performance is best if the clock rise and fall times are 4 ns or less.

If the **CLK** signal is interrupted, or its frequency is too low, the charge on internal capacitors can dissipate to the point where the accuracy of the output data will degrade. This is what limits the minimum sample rate.

The duty cycle of the clock signal can affect the performance of the A/D Converter. Because achieving a precise duty cycle is difficult, this device is designed to maintain performance over a range of duty cycles. While it is specified and performance is guaranteed with a 50% clock duty cycle, performance is typically maintained over a clock duty cycle range of 45% to 55%.

Applications Information (Continued)

The clock line should be series terminated at the source end in the characteristic impedance of that line. Use a series resistor right after the source such that the source impedance plus that series resistor equals the characteristic impedance of the clock line. This resistor should be as close to the source as possible, but in no case should it be further away than

$$\frac{t_r}{6 \times t_{PR}}$$

where t_r is the rise time of the clock signal and t_{PR} is the propagation rate down the board. For a Board of FR-4 material, t_{PR} is typically about 150 ps/inch.

To maintain a consistent impedance along the clock line, use stripline or microstrip techniques (see Application Note AN-1113) and avoid the use of through-holes in the line.

It might also be necessary to terminate the ADC end of the clock line with a series RC to ground such that the resistor value equals the characteristic impedance of the clock line and the capacitor value is

$$C \geq \frac{4 \times t_{PR} \times L}{Z_O}$$

where t_{PR} is again the propagation rate down the clock line, L is the length of the line in inches and Z_O is the characteristic impedance of the clock line.

5.0 LAYOUT AND GROUNDING

Proper routing of all signals and proper ground techniques are essential to ensure accurate conversion. Separate analog and digital ground planes are required to meet data sheet limits. The analog ground plane should be low impedance and free of noise from other parts of the system.

Each bypass capacitor should be located as close to the appropriate converter pin as possible and connected to the pin and the appropriate ground plane with short traces. The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (e.g., a filter capacitor) connected between the converter's input and ground should be connected to a very clean point in the analog ground return.

Figure 7 gives an example of a suitable layout, ground plane separation, and bypass capacitor placement. All analog circuitry (input amplifiers, filters, reference components, etc.) should be placed on or over the analog ground plane. All digital circuitry and I/O lines should be over the digital ground plane.

Digital and analog signal lines should never run parallel to each other in close proximity with each other. They should only cross each other when absolutely necessary, and then only at 90˚ angles. Violating this rule can result in digital noise getting into the input, which degrades accuracy and dynamic performance (THD, SNR, SINAD).

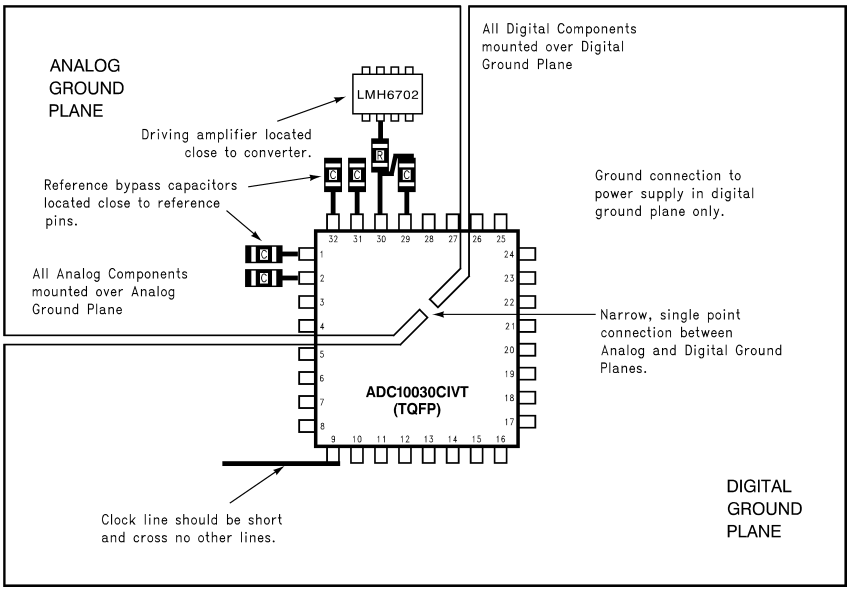


FIGURE 7. An Acceptable Layout Pattern for the ADC10030

Applications Information (Continued)

6.0 DYNAMIC PERFORMANCE

The ADC10030 is ac tested and its dynamic performance is guaranteed. To meet the published specifications, the clock source driving the CLK input must be free of jitter. For best ac performance, isolating the ADC clock from any digital circuitry should be done with adequate buffers, as with a clock tree. See *Figure 8*.

Meeting dynamic specifications is also dependent upon keeping digital noise out of the input, as mentioned in Sections 1.0 and 5.0.

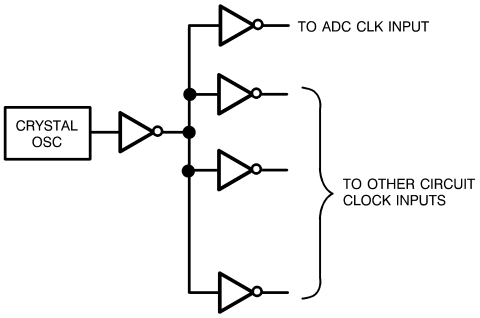


FIGURE 8. Isolating the ADC Clock from Digital Circuitry

7.0 COMMON APPLICATION PITFALLS

Driving the inputs (analog or digital) beyond the power supply rails. For proper operation, all inputs should not go more than 300 mV beyond the supply pins. Exceeding these limits on even a transient basis can cause faulty or erratic operation. It is not uncommon for high speed digital circuits (e.g., 74F and 74AC devices) to exhibit undershoot that goes more than a volt below ground. A resistor of 50Ω to 100Ω in series with the offending digital input will usually eliminate the problem.

Care should be taken not to overdrive the inputs of the ADC10030 (or any device) with a device that is powered from supplies outside the range of the ADC10030 supply. Such practice may lead to conversion inaccuracies and even to device damage.

Attempting to drive a high capacitance digital data bus. The more capacitance the output drivers has to charge for each conversion, the more instantaneous digital current is required from V_D I/O and DGND I/O. These large charging current spikes can couple into the analog section, degrading dynamic performance. Adequate bypassing and maintaining separate analog and digital ground planes will reduce this problem on the board. Buffering the digital data outputs (with an 74F541, for example) may be necessary if the data bus to be driven is heavily loaded. Dynamic performance can also be improved by adding series resistors of 47Ω at each digital output.

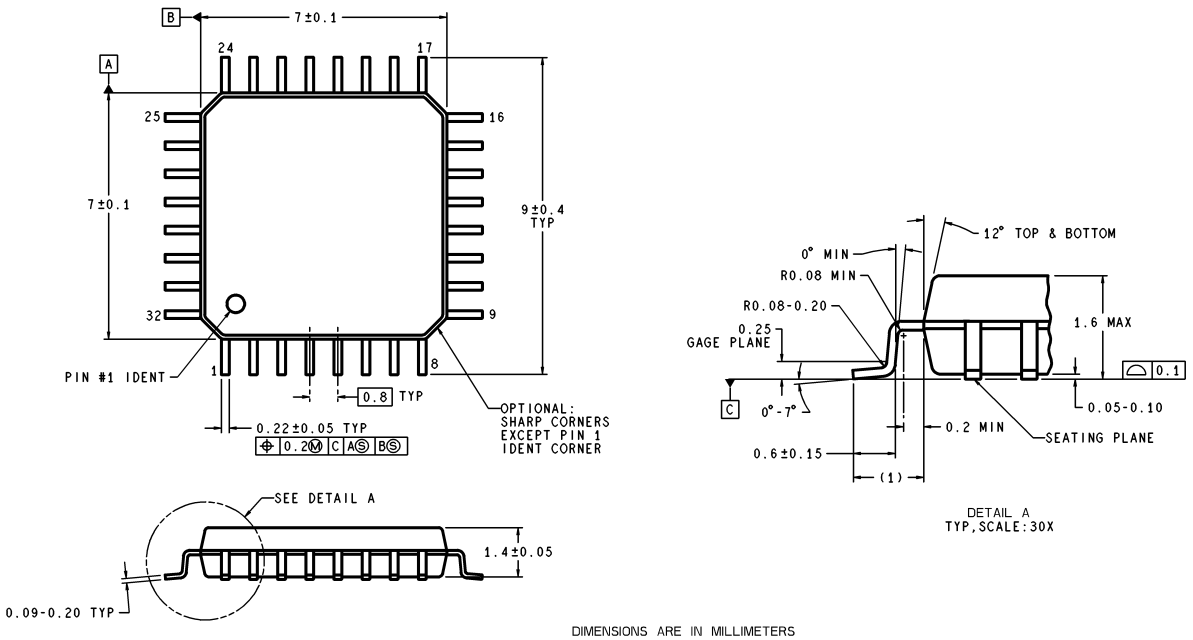
Driving the V_{REF}+ F pin or the V_{REF}– F pin with devices that can not source or sink the current required by the ladder. As mentioned in section 2.0, be careful to see that any driving devices can source sufficient current into the V_{REF}+ F pin and sink sufficient current from the V_{REF}– F pin. If these pins are not driven with devices than can handle the required current, they will not be held stable and the converter output will exhibit excessive noise.

Using a clock source with excessive jitter. This will cause the sampling interval to vary, causing excessive output noise and a reduction in SNR performance. The use of simple gates with RC timing is generally inadequate.

Using the same voltage source for V_D and digital logic. As mentioned in section 3.0, V_D should use the same power source used by V_A, but should be decoupled from V_A.

Physical Dimensions inches (millimeters)

unless otherwise noted



DIMENSIONS ARE IN MILLIMETERS

VBE32A (Rev E)

32-Lead TQFP Package
Ordering Number ADC10030CIVT
NS Package Number VBE32A

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